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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/672,223	09/27/2000	Yun-Sang Lee	AB-1043 US	6183

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EXAMINER	
CHAUDRY, MUJTABA M	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/672,223	LEE, YUN-SANG	
	Examiner	Art Unit	
	Mujtaba K Chaudry	2133	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14-16 and 18-21* is/are pending in the application.

4a) Of the above claim(s) *13 and 17* is/are withdrawn from consideration.

5)☒ Claim(s) *2,4,9-12 and 18-21* is/are allowed.

6)☒ Claim(s) *1,3,5-8 and 14-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 9/27/00 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

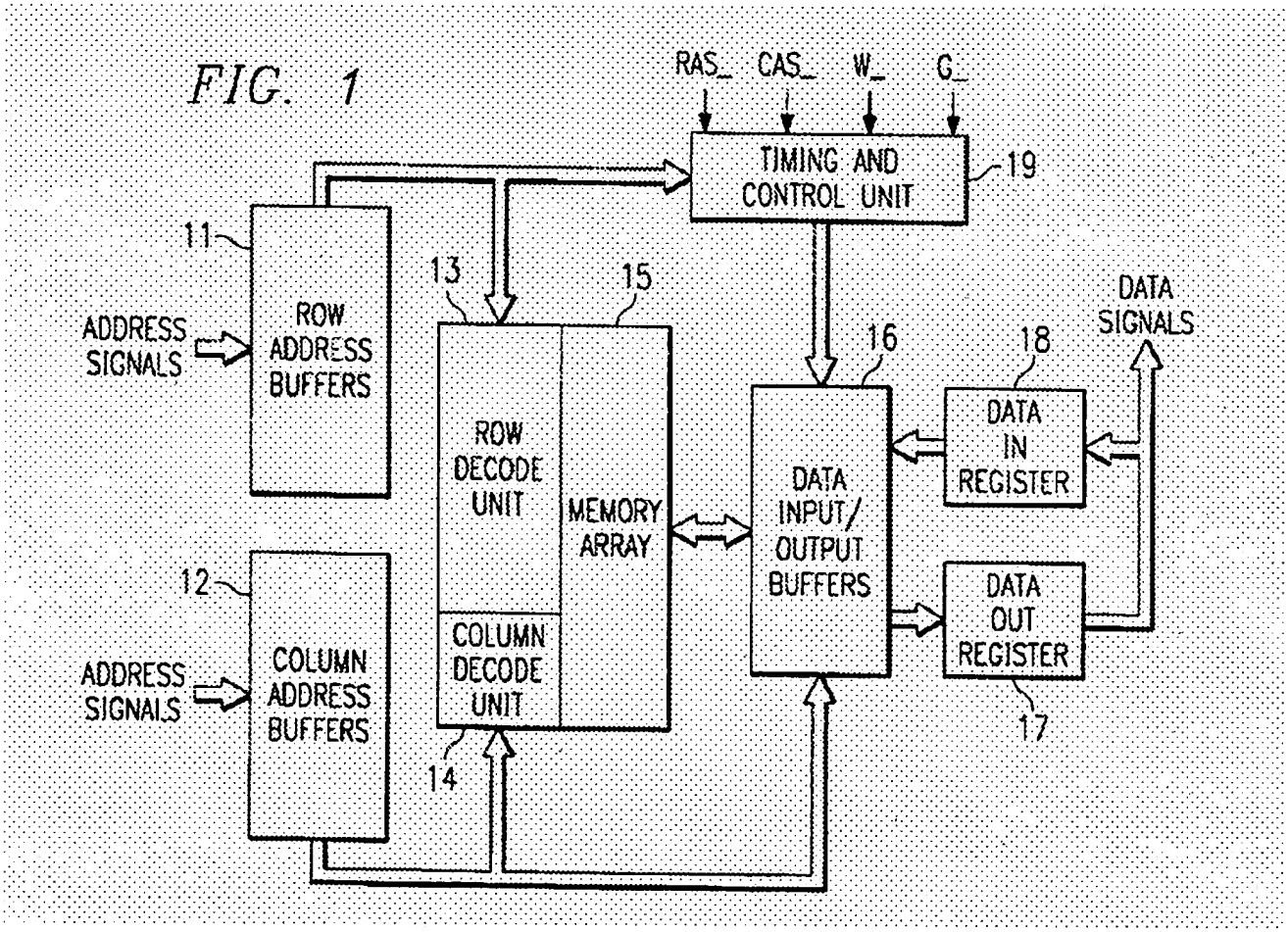
Response to Amendment

Applicant's arguments/amendments with respect to previously presented claims 1-12, 14-16 and 18-20, cancelled claims 13 and 17, and newly added claim 21 filed January 6, 2005 have been considered but are not fully persuasive. In light of newly presented arguments and search, the Examiner hereby suggests claims 2, 4, 9-12 and 18-21 to be in condition for allowance. Hence the application will be forwarded for allowance pending the cancellation of claims 1 and 3 with all depending claims.

Applicant contends, "...Surlekar (prior art of record) fails to disclose or suggest a selection circuit for controlling transfer paths of the internal signals and data in response to selection signals..." The Examiner respectfully disagrees. Surlekar teaches (Figure 1) a block diagram of a semiconductor memory unit. In the memory unit, ADDRESS SIGNALs are applied to row address buffers 11 and to column address buffers 12. The ADDRESS SIGNALs stored in the row address buffers 11 are applied to the row decode unit 13 and to the timing and control unit 19, while the ADDRESS SIGNALs stored in the column address buffers are applied to the column decode unit 14 and to the data input/output buffers 16. The signals from the row decode unit 13 and the column decode unit 14 are applied to the memory array 15, the signals applied to the memory array 15 specifying a group of memory array cells to be manipulated in response to control signals. Control signals are applied to the timing and control circuit 19. The control signals include the ROW ADDRESS STROBE.sub.-- (RAS.sub.--), the COLUMN ADDRESS STROBE.sub.-- (CAS.sub.--), the WRITE ENABLE.sub.-- (W.sub.--), and the OUTPUT

ENABLE.sub.-- (G.sub.--). (The convention being used herein is that the .sub.-- symbol following a signal name indicates the logical complement of the signal.) Output signals from the timing and control unit 19 are applied to the data input/output buffers 16. The memory array unit 15 applies signals to, and receives signals from, the data input/output buffers 16. The data input/output buffers 16 receive signals from the data in register 18 and applies signals to the data out register 17. DATA SIGNALs are applied to the data in register and are received from the data out register 17.

FIG. 1



Reasons for Allowable Subject Matter

Claims 2, 4, 9-12 and 18-21 are allowed. The following is an Examiner reasoned statement:

Independent claim 2 of the present application teaches an integrated circuit device comprising: a plurality of internal circuits for generating a plurality of internal signals, the internal signals used for addressing storage locations and for controlling internal operations; a first selection circuit for receiving the internal signals in response to selection signals corresponding to test information signals; a second selection circuit for receiving output signals from the first selection circuit and output signals from a sense amplifier, and for opening an alternative one of transfer paths for the internal signals and output signals and the output signals of the sense amplifier in response to the selection signal and a data output buffer for transferring output signals from the second selection signals externally from the integrated circuit device through data input/output pads, the data input/output pads being shared by the internal signals and the output signals from the sense amplifier. The foregoing limitations are not found in the prior arts of record. The prior art of record, namely Surlekar, teaches a memory unit having an array of storage cells which has been divided into groups of storage cells, by performing processing functions and, especially the comparison function, in the vicinity of each group of storage cells which are under test. The testing procedure involves the storage of a selected logic signal, referred to as the expected data signal, in each addressable cell, the retrieval of the stored logic signal from each storage cell, and the comparison of the retrieved data signal with the expected data signal (supplied by the user) to verify that the storage into and retrieval from the storage cells provides the signal that was originally stored in the memory unit. None of the prior arts of record teach nor fairly suggest all the limitations in the independent claim 2 of the present

application. In particular, the limitations of "...a second selection circuit for receiving output signals from the first selection circuit and output signals from a sense amplifier, and for opening an alternative one of transfer paths for the internal signals and output signals and the output signals of the sense amplifier in response to the selection signal..." are not taught or fairly suggested in the prior arts of record. Therefore independent claim 2 is allowed.

Independent claim 4 recites similar limitations of independent claim 2 and therefore is allowed for similar reasons.

Dependent claims 9-12 and 18-21 depend from independent claims 2 and 4 and inherently include limitations therein and therefore are allowed as well.

Conclusion

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
January 18, 2005

Guy J. Lamarre
Primary Examiner